EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Frederick E. Cooperrider on 7/9/2009.

2. Please amend the claims filed in the supplemental amendment filed 7/7/2009 as follows. Note that this supplemental amendment further amends the claims filed on 6/8/2009, which had not been previously entered.

The specification amendment filed 7/9/2009, which fixes a typographical issue with the previously filed specification amendment filed 7/7/2009 (k=2 is now underlined to show it is newly amended), is also entered.

3. Please amend claim 1 as follows:

a. In line 20, please amend "aid" to read "said" in view of the inadvertent strikethrough.

b. In line 28, please remove extra spaces such that "streams ," is amended to read "streams,".

4. Please amend claim 11 as follows:

c. In line 1, please delete the limitation “said”.

5. Please amend claim 12 as follows:

d. In line 29, please change ”matrix multiplication” to “linear algebra”.

e. In line 31, please change “level 3 processing” to “level 3 linear algebra processing”.

REASONS FOR ALLOWANCE

6. The following is an examiner’s statement of reasons for allowance.

Prior art of record does not teach selecting, from a plurality of six kernels, two kernels to use for executing said level 3 processing, said six kernels having different prefetch patterns, said six kernels adapted to perform said level 3 processing using said register block format, and whereby said two kernels are selected so that said data copy processing during said level 3 processing is not necessary…said three data streams…resident in said caches and main memory as dictated by a logic of said two kernels, in the context of the other remaining limitations of the claim. In addition, the appropriate terminal disclaimers have been filed to preclude otherwise applicable double patenting rejections.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

f. Taylor (US 5206822) discloses of optimizing processing of sparse matrices by storing matrices in a special compact format.

g. Myszewski (US 5099447) discloses of matrix multiplication for computers with hierarchical memory.

h. Razdow (US 5771392) discloses of data structures that could be used to represent nested matrices.

i. Gilbert et al. (US 5781779) discloses of generating computationally efficient program code for carrying out computations on matrix data using data structures.

j. Pingali et al. (US 6357041) discloses of using control-centric transformations to modify the control flow of a program to improve data locality in matrix multiplication.

k. Macy (US 20040122887) discloses of efficient multiplication of small matrices using SIMD registers.

l. Wadleigh (US 7028168) discloses of storing partitioned matrices in a contiguous memory workspace to reduce the occurrence of cache misses.

m. Lumsdaine et al. (US 20070198621) discloses of storing matrices in a format to improve overall computational performance.

n. Spracklen (US 20030221089) discloses of a data manipulation matrix module in which SIMD instructions manage operand data element alignment.

o. Pinar et al. (Improving Performance of Sparse Matrix-Vector Multiplication) discloses of alternative data structures to improve performance and alleviate poor cache utilization and extra load operations.

p. Herrero (New Data Structures for Matrices and Specialized Inner Kernels: Low Overhead for High Performance) discloses of using new data structures for dense linear algebra codes to improve locality, avoid data copies, and obtain reduced storage requirements. Also disclosed is defining and using simpler kernels when NDS are used, and avoiding data copies. Of particular reference is a list of citations which follow this approach on the second page.

q. Bader et al. (Cache Oblivious Matrix Operations Using Peano Curves) discloses of the concept of storing matrix elements in a certain order to foster an algorithm with excellent locality features.

r. Anderson et al. (A Fully Portable High Performance Minimal Storage Hybrid Format Cholesky Algorithm) discloses of using a hybrid format where blocks of the matrices are held contiguously and which avoids data copies inevitable when Level-3 Blas are applied to conventionally stored matrices.

s. Gunnels et al. (A New Array Format for Symmetric and Triangular Matrices) discloses of a new data format for storing certain matrices, and data

format conversion routines between the conventional formats and the new data format.

t. Anderson et al. (A Recursive Formulation of Cholesky Factorization of a Matrix in Packed Storage) discloses of transforming a matrix from standard packed format to a new format.

u. Gustavson et al. (New Generalized Data Structures for Matrices Lead to a Variety of High Performance Algorithms) discloses of new data structures based on the benefits of arrays which are contiguous and properly aligned.

v. Chatterjee et al. (Nonlinear Array Layouts for Hierarchical Memory Systems) discloses of increased performance when algorithmic patterns of locality of reference match the patterns that the cache organization supports well, e.g. restructuring multidimensional arrays to be "cache-conscious" or "memory-friendly" and altering the default row-major and column-major linearization of the aforementioned arrays. Further disclosed are nonlinear array layouts.

w. Gustavson et al. (Recursive Blocked Data Formats and BLAS's for Dense Linear Algebra Algorithms) discloses of new data formats for maintaining data locality at every level of the memory hierarchy and hence providing high performance on memory tiered processors.

x. McKellar et al. (Organizing Matrices and Matrix Operations for Paged Memory Systems) discloses carefully designed matrix algorithms and matrix representations can minimize page faulting.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 5:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Keith Vicary/
Examiner, Art Unit 2183